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		EXAMINER		
		PSITOS, ARISTOTELIS M		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/840,091	Applicant(s) HAUSBERGER ET AL.	
	Examiner Aristotelis M. Psitos	Art Unit 2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 May 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

Art Unit: 2627

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The IDS has been received and made of record.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

Claim 13 refers to "the signal bridge", but such is not defined in claim 1.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Art Unit: 2627

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1,2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al further considered with Cini, further considered with the Finck et al article and all further considered with Stevenson et al and all further considered with Yamaguchi.

Oh et al disclose an optical read-out system having modular components/units, see for instance rf module 24, av decoder 24, microprocessor 20, etc. Although the RF module fails to describe an appropriate amplifier therein, Cini teaches IC amplifiers. As further recognized by the Finck et al article decoder ics are also well known.

Stevenson teaches that chip sets can be "plugged in" to a board. Yamaguchi teaches motherboard with appropriate daughter boards connected thereto.

The examiner concludes that it would have been obvious to one of ordinary skill in the art to arrange upon a "mother board", pluggable additional circuits, chips/ic sets, such as amplifiers, decoders, etc. Such modular construction permits easy trouble shooting of elements, as well as arrangement of the circuits to fit particular physical dimensions as required. The examiner interprets the RF module as also having an amplifier.

With respect to claim 2, the amplifier is present, to arrange such that the amplifier and optical scanning device are in a unified "module" Is considered merely a design configuration, i.e., placing of selected components in stand-alone packages. No unobvious results are seen to occur from such an arrangement.

With respect to claim 3, again, the inclusion of the decoder ic/chip along with the control device, such as the microprocessor of Oh et al is an arrangement of components and considered obvious to those of ordinary skill in the art – an arrangement of parts.

With respect to claim 4, separate modules for each of the signal processor, amplifier and decoder is considered present in Oh et al – see the separate elements discussed above.

Art Unit: 2627

With respect to claim 5, terminals associated with individual electronic devices are well known. As depicted in Oh et al there is a plurality of output terminals/lines from the amplifier. Hence the appropriate terminals are considered present in Oh et al.

With respect to claim 6, similarly the provision of the microcontroller in Oh et al/processor on its own module/circuit board/daughter board appropriately connected to a main mother board is considered obvious, i.e., the placement of electronic modules, such as a processor/controller on its own "daughter board" and connecting such to a "mother board".

With respect to claim 7, terminals are required (in/out) terminals/lines, and hence necessary for the system to operate, i.e., be electronically connectable.

With respect to claim 8, the selection of which module is on a "daughter board" is merely an exercise in configurations, and no unexpected results are seen to occur therefrom.

With respect to claim 12, such plug-on chip is met.

With respect to claim 13, real-time controller elements/microprocessors, etc are considered part of the circuit arrangement of the Finck et al article – see figure 3, control processor.

With respect to claim 17, such printed circuit boards are present above.

With respect to claim 23, a common mount for all the modules is interpreted as a "mother board". The ability of having a "mother board" for a plurality of circuits/printed/chips/ sometimes referred to as "daughter" boards is present above in Yamaguchi et al.

5. Claims 9,10, 11,14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the art as applied to claim 1 above, and further in view of Engels et al.

Engels et al teach a modular constructed evaluation system wherein an input unit/detector head is connected to additional electrical circuit elements – see figure 4, and the appropriate elements, plurality of amplifiers (parallel circuit arrangement), adc/fpga units, and additional components such as an Ethernet connection.

Art Unit: 2627

With respect to claim 11, the examiner interprets the rf module of Oh et al providing for a continuous signal bridge to the remaining components/units/modules therein. Furthermore, as additional disclosed/depicted in Engels et al – see the pci bridge element in figure 9.

It would have been obvious to modify the base systems as relied upon above with respect to claim 1 and further modify such with the above noted teachings from Engels et al, motivation is to provide for appropriate parallel circuit arrangements for yielding a digital module – as noted in col. 2, starting at line 25.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the art as applied to claim 1 above, and further in view of Ulrich et al.

Ulrich et al discloses a hard disc drive tester/portable. This unit – element 101 has internal testing cards. Furthermore, the unit has additional interface connection through element 105 for subsequent connection to a variety of elements.

It would have been obvious to modify the base systems as relied upon above with respect to claim 1 and further modify such with the above teachings from Ulrich et al, motivation is to provide for a testing unit with additional connection/terminal to external “measuring” cards.

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the art as applied to claim 17 above, and further in view of Maxwell.

The use of metal for a rack, in which circuit boards are connected is well known as taught by Maxwell.

It would have been obvious to modify the base systems as relied upon above with respect to claim 17 and modify such with the above noted rack teaching, motivation is to provide for a strong supporting mount.

8. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al further considered with Cini, further considered with the Finck et al article and all further considered with Stevenson et al and all further considered with Yamaguchi and all further considered with Mickieviez et al.

Art Unit: 2627

The references to Oh et al, Cini, the Finck et al article, Stevenson et al, and Yamaguchi and all are relied upon for the reasons stated above with respect to claim 1.

Th Mickieviez et al further teaches the appropriate vertical arrangement of circuit boards in this environment.

It would have been obvious to modify the base systems with the additional teaching from Mickieviez et al, motivation is to permit closer spacings between circuit boards in a common housing.

With respect to claim 20, separate circuit boards/printed circuits is considered obvious in view of Oh et al which depicts various separate circuit components separately. The ability of providing such separate boards in modular construction is considered well known for ease of trouble shooting defective components.

With respect to claims 22 and 23, the arrangement of the individual circuit boards is considered merely an exercise is circuit arrangement and obvious to those of ordinary skill in this art, especially because no unexpected results are seen/disclosed to occur from such an arrangement.

Conclusion

Butler et al is cited as illustrative of a disc inspection device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristotelis M. Psitos whose telephone number is (571) 272-7594. The examiner can normally be reached on M-F: 6:00 - 2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dwayne D. Bost can be reached on (571) 272-7023. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2627

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aristotelis M Psitos
Primary Examiner
Art Unit 2627

A handwritten signature in black ink, consisting of a series of loops and flourishes, positioned to the right of the printed name and title.

AMP